



## **Altera's RapidIO IP Core Qualified to RIOLAB Level 3 Device Interoperability**

*DIL- Qualification Provides Customers a Greater Level of Confidence When Designing Altera's FPGAs into a RapidIO System*

**Ottawa, Canada – July 23,, 2009** – RIOLAB™, a division of Fabric Embedded Tools Corporation and the world's only independent RapidIO® interoperability testing facility, today announced Altera's RapidIO MegaCore® function IP, version 9.0, successfully completed the third level of RIOLAB's Device Interoperability Level (DIL) testing. RIOLAB DIL qualified Altera's RapidIO IP core using a Stratix® II GX FPGA.

Altera's RapidIO MegaCore Function is available across Altera's mid-range and high-end device series, including its latest 40-nm portfolio consisting of Stratix IV FPGAs, Arria® II GX FPGAs and HardCopy® IV ASICs.

"Altera's qualification of their RapidIO IP within an FPGA to DIL-3 is an excellent endorsement of the capability of their IP. DIL-3 Interoperability reports represent the completion of the Device Interoperability test suite and has become an increasingly required milestone of achievement before OEMs can consider RapidIO devices for new designs." said Jim Parisien, president of Fabric Embedded Tools.

RIOLAB tests, based on the RapidIO Trade Association's "RapidIO Device Interoperability and Specification Compliance Checklists, 1.3 Spec," address the graduated levels of interoperability that align with the increasing complexity of both the RapidIO specification and the needs of silicon vendors and OEMs.

DIL-1 tests verify device support for initialization, enumeration and basic read and write packet transactions. In DIL-1 testing, the device-under-test is tested against the entire RIOLAB hardware library for both request and response level transactions, with an emphasis on the reliability of interaction between devices. DIL-2 testing is the first level that delves deeper into register and packet protocol





compliance under a variety of conditions that are not covered within DIL-1. DIL-3 is the final stage of device interoperability testing as defined within the RapidIO Trade Association specification compliance checklist.

"As one of the first IP vendor to reach a DIL-3 level of interoperability, Altera has demonstrated their leadership and interest in building a solid reputation around the RapidIO ecosystem. Interoperability Reports from RIOLAB continue to be fundamental tools for OEMs to determine how well a RapidIO device and/or IP functions in a real system environment and with multi-vendor switches and endpoints," said Tom Cox, executive director of the RapidIO Trade Association.

### **About Fabric Embedded Tools**

Fabric Embedded Tools Corporation (<http://www.fetcorp.com>) is the leading provider of RapidIO software, network management and diagnostic tools. The company delivers innovative solutions that shorten product development and testing cycles, and reduce technology risks and time-to-market. Through its unwavering commitment to delivering powerful, time-saving tools and services, excellence in customer support, and strong partner relationships, FET meets the needs of semiconductor vendors, single board computer vendors, and OEMs across the embedded industry.

A division of Fabric Embedded Tools, RIOLAB ([www.riolab.com](http://www.riolab.com)), is a state-of-the-art RapidIO interoperability testing facility that provides device interoperability and specification compliance reports that meet the growing needs of silicon vendors and OEMs designing with RapidIO technology. The lab is the only facility in existence that provides commercial semiconductor vendors, FPGA and ASIC manufacturers with an unbiased common vehicle for demonstrating device interoperability and specification compliance to the RapidIO standard.

For more information contact:

[info@fetcorp.com](mailto:info@fetcorp.com)

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