

Xilinx RapidIO LogiCORE IP Achieves RIOLAB Level 1 and Level 2 Device Interoperability Qualification

DIL- Qualification Provides Customers a Greater Level of Confidence When Designing Xilinx's FPGAs into a RapidIO System

Ottawa, Canada – July 28, 2009 – RIOLAB™, a division of Fabric Embedded Tools Corporation and the world's only independent RapidIO® interoperability testing facility, today announced Xilinx's RapidIO Endpoint LogiCORE™ IP, version 5.1, successfully completed the first two levels of RIOLAB's Device Interoperability Level (DIL) testing. RIOLAB DIL qualified Xilinx's RapidIO IP using a Virtex5® FPGA.

Xilinx RapidIO LogiCORE IP, designed to RapidIO Interconnect specification version 1.3, is available on Xilinx Virtex®-4, Virtex®-5, and Virtex®-6 FPGA devices and support 1x and 4x lane width at 1.25G, 2.5G, and 3.125G line rates. The low cost and flexible IP solution allows application specific parameterization and configuration at Physical layer, Logical (I/O) and Transport Layer, and data buffers to facilitate optimal and low cost design. The data buffers can be configured to be 8, 16, or 32 packet deep in order to accommodate varied data traffic profiles requirements. Xilinx RapidIO IP is high quality and reliable design, and is widely deployed in the industry.

"The qualification of RapidIO IP to DIL-2 is a significant achievement. It demonstrates to customers a confidence and commitment that Xilinx has in the quality of their IP and a willingness to enable customers with independent 3rd party testing reports," said Jim Parisien, president of Fabric Embedded Tools. "Interoperability reports are a very effective tool in helping developers make informed decisions that will lead them towards success with their next RapidIO design.

RIOLAB tests, based on the RapidIO Trade Association's "RapidIO Device Interoperability and Specification Compliance Checklists, 1.3 Spec," address the graduated levels of interoperability that align with the increasing complexity of both the RapidIO specification and the needs of silicon vendors and OEMs.

DIL-1 tests verify device support for initialization, enumeration and basic read and write packet transactions. In DIL-1 testing, the device-under-test is tested against the entire RIOLAB hardware library for both request and response level transactions, with an emphasis on the reliability of interaction between devices. DIL-2 testing is the first level that delves deeper into register and packet protocol compliance under a variety of conditions that are not covered within DIL-1. The prerequisite for DIL-2 testing is proof of successfully passing DIL-1.

"Xilinx has been committed to RapidIO since its inception. This latest RIOLAB achievement is one more key step to demonstrating this continued commitment to quality RapidIO IP," said Harpinder S Matharu, Senior Marketing Manager, Xilinx Inc. "RIOLAB DIL-1 and DIL-2 qualification provides our customers a greater level of assurance that our RapidIO solutions are interoperable within the RapidIO ecosystem."

"With the introduction of more and more choices for RapidIO processing endpoints, customers are faced with a growing need for clear, unbiased facts on which to base their decisions", said Tom Cox, Executive Director of the RapidIO Trade Association.

"Interoperability Reports from RIOLAB are fundamental tools for OEMs to determine how well a RapidIO device can function in their next system."

About Fabric Embedded Tools

Fabric Embedded Tools Corporation (<http://www.fetcorp.com>) is the leading provider of RapidIO software, network management and diagnostic tools. The company delivers innovative solutions that shorten product development and testing cycles, and reduce technology risks and time-to-market. Through its unwavering commitment to delivering powerful, time-saving tools and services, excellence in customer support, and strong partner relationships, FET meets the needs of semiconductor vendors, single board computer vendors, and OEMs across the embedded industry.

A division of Fabric Embedded Tools, RIOLAB (www.rio-lab.com), is a state-of-the-art RapidIO interoperability testing facility that provides device interoperability and specification compliance reports that meet the growing needs of silicon vendors and OEMs designing with RapidIO technology. The lab is the only facility in existence that provides

commercial semiconductor vendors, FPGA and ASIC manufacturers with an unbiased common vehicle for demonstrating device interoperability and specification compliance to the RapidIO standard.

For more information contact:

finfo@fetcorp.com

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